SUBMISSION OF TERMINAL DISCLAIMER:

Submitted herewith is a terminal disclaimer disclaiming the terminal part of any patent granted on this application which would extend beyond the expiration date of U.S. Patent No. 6,713,325.

IN THE SPECIFICATION:

The Cross Reference to Related Applications on page 1 has been amended as follows:

The present application is a division of ~~based on prior U.S.~~ Application Serial No. 10/267,365, filed on October 9, 2002, now U.S. Patent No. 6,713,325, which is hereby incorporated by reference, and priority thereto for common subject matter is hereby claimed.

Paragraph beginning at line 12 of page 16 has been amended as follows:

Furthermore, as shown in FIG. 2B, in order to conduct deep ion implantation, for example, an embedded insulating film neighboring high-density N-type source region 143 and an embedded insulating film neighboring drain region 153 having a density of about $1E18/cm^3$ are formed at the energy of about 100 KeV. Next, as shown in FIG. 2C, the insulating film 16 overlying the source/drain regions and the gate electrodes is dry etched so as to form a sidewall 17 around the gate electrode 12. The sidewall 17 serves as an implantation mask when the implantation to the source and the drain is conducted in the later process. As best shown in Fig. 3B, the source regions 141-143 and the drain regions 151-153 constitute source extension regions and drain extension

regions, respectively, stacked in a thickness direction of the semiconductor film 1.